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10/673,138	09/30/2003	Andrej S. Mitrovic	236518US6YA	3830

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EXAMINER	
SAXENA, AKASH	
ART UNIT	**PAPER NUMBER**
2128	

SHORTENED STATUTORY PERIOD OF RESPONSE	NOTIFICATION DATE	DELIVERY MODE
3 MONTHS	04/20/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Notice of this Office communication was sent electronically on the above-indicated "Notification Date" and has a shortened statutory period for reply of 3 MONTHS from 04/20/2007.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/673,138	MITROVIC, ANDREJ S.	
	Examiner	Art Unit	
	Akash Saxena	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 January 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claim(s) 1-47 has/have been presented for examination based on amendment filed on 11th January 2007.
2. Claim(s) 1, 14, 21, 34, 39, 41, 42, and 44 is/are amended.
3. Claim(s) 44 remains rejected under 35 USC § 101.
4. Claim(s) 1-47 remain rejected under 35 USC § 103.
5. The arguments submitted by the applicant have been fully considered. Claims 1-47 remain rejected and this action is made FINAL. The examiner's response is as follows.

Response to Applicant's Remarks for 35 U.S.C. § 103

6. **Claims 1-47 were rejected under 35 U.S.C. 103(a) as being unpatentable over Sonderman, in view of Jain.**

Regarding Claims 1-47

(Argument 1)

Applicant has pointed to section cited by examiner, Sonderman Col.9 Lines 45-61, and argued:

> Sonderman Col.9 Lines 45-61
> The system 100 then optimizes the simulation (described above) **to find more optimal process target (Ti)** for each silicon wafer, Si to be processed. These target values are then used to generate new control inputs, XTi, on the line 805 to control a subsequent process of a silicon wafer Si. The new control inputs, XTi, are generally based upon a plurality of factors, such as simulation data, output requirements, product performance requirements, process recipe settings based on a plurality of processing tool 120 operating scenarios, and the like. [emphasis added]

Stating:

> Thus, this section of Sonderman et al. clearly discloses that the simulation is to find a more optimum process target for each silicon wafer **to be processed**. The simulation results produce a new control input for the silicon wafer **to be processed**. Thus, Applicant respectfully submits that Sonderman et al. teach performing first principles simulation for the actual process being performed before performance of the actual process, and not the claimed performing first principles simulation for the actual process being performed during performance of the actual process. Thus, Sonderman et al. do not disclose and indeed teach away from the present invention. For at least this reason, Applicant submits that the present invention patentably defines over Sonderman et al.2

Where Sonderman does not teach the limitations:

> performing first principles simulation for the actual process being performed during performance of the actual process using the physical model to provide a first principles simulation result in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed; and
>
> using the simulation result obtained during the performance of the actual process as part of a data set that characterizes the actual process being performed by the semiconductor processing tool.

(Response 1)

Applicant alleges that, "Sonderman et al. teach performing first principles simulation for the actual process being performed before performance of the actual process and not the claimed performing first principles simulation for the actual process being performed during performance of the actual process."

The deficiency in the argument relates to Sonderman *teaching away* from performing concurrent simulation and actual processing. As asserted earlier, there is no such disclosure in Sonderman, and all the facts point towards, contrary to applicant's assertion of teaching away, that the simulation can be performed with actual process (Sonderman: Fig.1-3) and sequentially with feedback to the actual process for the subsequent processes/wafers (Sonderman: Col.9 Lines 45-61). Examiner finds applicant's arguments unpersuasive.

(Argument 2 & Response 2)

Further applicant has argued that *Jain reference does not teach or suggest first principle simulation* (non-enabled), as it is speculative. The claim limitation require "inputting first principle simulation model...", "performing first principle simulation..." and using "first principle simulation results...". Applicant is arguing that the cited paragraph in Jain is a proposed (not enabled) wafer scale mathematic Physical Engine (MPE) implementation proposed to solve the first principle simulation. *Examiner asserts that applicant's are arguing limitation more specifically than the claims require. Specifically, they are arguing the implementation of the first principle model, whereas none of that is claimed*. The teaching of Jain clearly teaches the claimed limitation. Even if for argument sake, wafer scale implementation of the

MPE engine is not enabled, the simulation concept (to perform MPE simulation of physical phenomenon) and other embodiments to implement the simulation concept (Pg. 370-372 – Sections III and IV) are disclosed. The important fact is that Jain teaches MPE to solve the physical phenomenon ranging from fluid flow to electromagnetic field dynamics to thermal patterns inside a semiconductor wafer (Abstract first line), and includes embodiments to do so. Enablement of the MPE engine in any embodiment will meet the claimed limitation. Examiner finds applicant's argument unpersuasive and maintains the rejections for independent claims 1, 23, 45 and 48.

(Argument 3)

Applicant has argued for claim 16, that Sonderman discloses Advanced Process Control (APC) on a factory wide basis, but there is no disclosure of using network of interconnected resources inside the semiconductor device manufacturing facility to perform first principle simulation as defined in claim 1. Jain discloses interconnected resources, but they are at geographically displaced sites.

(Response 3)

Examiner finds applicant's argument unpersuasive, as there is no limitation that specifically requiring network resources not be geographically displaced. Further, even if claimed, that would be advancement on the localized resources, as it would require more technical and innovative expertise to co-ordinate such a simulation. Secondly, in response to, Sonderman not teaching network of interconnected resources inside the semiconductor device manufacturing facility to perform first

principle simulation, Jain reference is used to teach networked first principle simulation. Sonderman clearly teaches semiconductor simulation (Sonderman: Fig.1). As to interconnected resources, Sonderman states

> Sonderman Col.9 Lines 58-65:
> "In some embodiments, the APC can be a factory-wide software system; therefore, the control strategies taught by the present invention can be applied to virtually any of the semiconductor manufacturing tools on the factory floor"

One of ordinary skill in the art would have known that, to virtually apply control strategies to any semiconductor-manufacturing tool on the factory floor, it would require them to be networked/interconnected. Claims 16, 38 and 46 remain rejected. Applicant's argument regarding establishing a prima facie case of obviousness are considered and are found to be unpersuasive.

Claim Rejections - 35 USC § 112¶1st and response the applicant's remarks

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claim 1-51 are rejected under 35 U.S.C. 112, first paragraph, as based on a disclosure which is not enabling. Exact details of what basic physical and chemical attribute of the semiconductor processing tool are used to construct a first principle simulation model which is critical or essential to the practice of the invention, but not included in the claim(s) is not enabled by the disclosure. See *In re Mayhew*, 527 F.2d 1229, 188 USPQ 356 (CCPA 1976).

Applicant has argued that the meaning of the basic physical and chemical attribute of the semiconductor-processing tool is discernable to one of ordinary skill in the art. Although, teaching in the Maeda reference is present in exemplary format of molding tool, it is not there for a semiconductor-processing tool and does showing the physical and chemical attribute of the semiconductor-processing tool. Further, neither claim not the disclosure presents physical and chemical attribute of the semiconductor-processing tool in form of the first principles models.

(Response to applicant's remarks)

Applicant has provided an exact support in disclosure for such attributes in the model. Applicant has incorrectly quoted specification paragraphs [0035] and [0036]. These paragraph are not enabling although they rely on the commercially available packages to model the various first principle simulation models, the details of the

model are absent from the specification. Examiner respectfully maintains the rejection.

Claim Rejections - 35 USC § 101 and response the applicant's remarks

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

8. Claims 44 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

Claim 44 discloses "computer readable medium" which is defined in the specification (Pg.32-33 [00103] Line1-9) to include tangible items ("non volatile media" and "volatile media") and items that are non-tangible ("transmission media"). Therefore the claim as whole is not directed towards a tangible medium. One possible suggested way to overcome this rejection is to replace "computer readable medium" with "non volatile media" and "volatile media". Transmission media (Carrier wave) is understood be non-statutory and rejected under current office practice.

(Response to applicant's remarks)

Applicant has amended "computer readable medium *encoded with computer program*" as curing the above deficiency because,

> "a claimed computer-readable medium encoded with a computer program is a computer element which defines structural and functional interrelationships between the computer program and the rest of the computer which permit the computer's functionality to be realized and is thus statutory."

Is found to be unpersuasive because a carrier wave can still be *encoded with computer program.*

Response to Applicant's Remarks for Double Patenting

9. Applicant's arguments relating to filing a terminal disclaimer for applications 10/673,501 and 10/673,583 are considered and double patenting rejection is maintained until a terminal disclaimer is filed.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 1-44 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,802,045 issued to Sonderman et al (Sonderman hereafter), in view of IEEE article "Mathematic-physical engine: parallel processing for modeling and simulation of physical phenomena" by Jain et al (Jain hereafter).

Regarding Claim 1 (Updated)

Sonderman teaches a method to facilitate a process performed by a semiconductor-processing tool (Sonderman: Summary, at least in Col.2 Lines 10-17;Col.3 Lines 45-49) by inputting process data relating to the process performed by the semiconductor-processing tool (Sonderman: at least in Col.3 Lines 50-67; Col.7 Lines 8-20). Further, Sonderman teaches inputting the first principle physical model relating to the semiconductor-processing tool describing at least one of a basic physical or chemical attributes (Sonderman: at least in Col.5 Lines 11-17; 49-67) as device physics model, a process model and an equipment model. Further, Sonderman teaches performing first principle simulation *for the actual process being performed* during performance of actual process *(Sonderman: Col.7 Lines 4-7; Col.3 Lines 56-63, Fig. 1-3)* using the physical model to provide simulation results in accordance with the process data relating to the actual process being performed in order to simulate the actual process being performed (Sonderman: at least in Col.5-7; at least Col.7 Lines 8-20). Further, Sonderman teaches using the simulation results *obtained during the performance of the actual process* (Sonderman: Fig. 1-3

Col.7 Lines 4-7; Col.3 Lines 56-63) to facilitate the actual process performed by the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 48-64; Fig.1-8).

Sonderman does not teach first principle model including a set of computer encoded differential equations.

Jain teaches computer encoded differential equations using MPE engine, which can be applied to wafer processing (Jain: Abstract). Jain also teaches dedicated and wafer level implementation of MPE engine to provide enhanced performance (Jain: Pg. 372 Section V Dedicated MPE).

It would have been obvious to one (e.g. a designer) of ordinary skill in the art at the time the invention was made to apply the teachings of Jain to Sonderman to solve differential equation for the semiconductor processing tool. Sonderman teaches building various models, which work in real-time feedback control simulating actual semiconductor modeling process (Sonderman: Fig.1; Col.7 Lines 8-20), while Jain makes possible by providing model-solving capacity in real time when differential equations are present in the model (like thermal patterns in semiconductor wafer model) (Jain: Abstract).

Regarding Claim 2

Sonderman teaches directly inputting the process data relating to the actual process performed by the semiconductor-processing tool from at least one of physical sensor (eg. Scatterometry data, overlay data, dimensional data) and a metrology tool physically mounted on the semiconductor-processing tool (Sonderman: at least in Col.4 Lines 31-48; Col.4-8; Fig.1, 7; Col.7 Lines 8-20).

Regarding Claims 3-5

Sonderman teaches indirectly inputting the process data relating to the actual process performed by the semiconductor-processing tool from one of the manual input devices and a database as manual fashion data retrieval and automatic data retrieval; inputting data recorded from the previous run; inputting the data set by a simulation operator ((Sonderman: at least in Fig.1-3 Col.1; Col.4-7; Col.7 Lines 8-20).

Regarding Claims 6-9

Sonderman teaches inputting process data relating to at least one of the physical characteristics of the semiconductor-processing tool and semiconductor tool environment, data relating to at east on of the characteristics and a result of a process performed by the semiconductor processing tool; inputting a spatially resolved model (as modified models) of the geometry of the semiconductor processing tool; inputting fundamental equations necessary to perform first principle simulation for the desired simulation result (Sonderman: at least in Col.5 Lines 10-18; Col.6 Lines 48-63; Col.9 (equations); Col.5-9; Fig 1-3; Col.7 Lines 8-20).

Regarding Claim 10

Sonderman teaches performing interaction concurrently between the simulation environment (first principle simulation) and the semiconductor-processing tool (Sonderman: Fig.2; Col.4 Lines 48-63).

Regarding Claims 11-13

Sonderman teaches performing first principle simulation not concurrently with the process performed; inputting data from at least one initial condition recorded from a previous process performed (Sonderman: at least in Col.5-8; Fig.3-4).

Regarding Claims 14-18 (Updated)

Sonderman teaches using a network of interconnected resources *inside the semiconductor manufacturing facility (Sonderman: Semiconductor tools on the factory floor – Col.9 Lines 60-65*) to perform *first principle simulation (Jain: Section III*) recited in claim 1; using code parallelization among interconnected computational resources to share the computational load of the first principle simulation; sharing simulation information among the interconnected resources to facilitate a process by the semiconductor-processing tool; sharing simulation results among the interconnected resources to reduce redundant execution of substantially similar first principle simulation by different resources; sharing information comprising model changes among the interconnected resources to reduce the redundant refinements of first simulation by different resources (Sonderman: Fig.1-3, computer code software is described in Col.9 Lines 58 onward; Col.5-8).

Regarding Claims 19-20

Sonderman teaches remote access to computational and storage resources (Sonderman: Col.9 Line 58-Col.10 Line 31) where in wide area network is art inherent.

Regarding Claim 21 (Updated)

System claim 21 discloses substantially similar limitations as method claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 22

System claim 22 discloses substantially similar limitations as method claim 2 and is rejected for the same reasons as claim 2.

Regarding Claims 23-25

System claims 23-25 disclose substantially similar limitations as method claims 3-5 and are rejected for the same reasons as claims 3-5.

Regarding Claims 26-29

System claims 26-29 disclose substantially similar limitations as method claims 6-9 and are rejected for the same reasons as claims 6-9.

Regarding Claim 30

System claim 30 discloses substantially similar limitations as method claim 10 and is rejected for the same reasons as claim 10.

Regarding Claims 31-33

System claims 31-33 disclose substantially similar limitations as method claims 11-13 and are rejected for the same reasons as claims 11-13.

Regarding Claims 34-38 (Updated)

System claims 34-38 disclose substantially similar limitations as method claims 14-18 and are rejected for the same reasons as claims 14-18.

Regarding Claims 39-40 (Updated)

System claims 39-40 disclose substantially similar limitations as method claims 19-20 and are rejected for the same reasons as claims 19-20. Change in dependency from claim 34 to 21 of claim 39 is noted.

Regarding Claim 41 (Updated)

System claim 41 discloses substantially similar limitations as method claim 1 and is rejected for the same reasons as claim 1.

Regarding Claim 42 (Updated)

System claim 42 discloses substantially similar limitations as method claim 15 and is rejected for the same reasons as claim 15. Sonderman teaches means for sharing *inside the semiconductor manufacturing facility (Sonderman: Semiconductor tools on the factory floor – Col.9 Lines 60-65*) the computation load as shown in claim 15 rejection.

Regarding Claim 43

System claim 43 discloses substantially similar limitations as method claim 16 and is rejected for the same reasons as claim 16.

Regarding Claim 44 (Updated)

System claim 44 discloses substantially similar limitations as method claim 1 and is rejected for the same reasons as claim 1.

Regarding Claims 45-47

Jain teaches use of Navier Stokes and other known simulation solutions for solving various simulation problems as initial condition (Jain: Pg. 367-368 Section

"Governing Rationale" Sub-Section A. Governing Equations). Sonderman also teaches initializing the models with input data (Sonderman: Col.7 Lines 8-20).

Conclusion

11. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Communication

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Akash Saxena whose telephone number is (571) 272-8351. The examiner can normally be reached on 9:30 - 6:00 PM M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini S. Shah can be reached on (571)272-2279. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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